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Common-Drain Flip-Chip GaAs FET Oscillators

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***Abstract*—GaAs FET oscillators with flip-chip mounted devices in a novel common-drain configuration are described. It is shown how common-drain oscillators can achieve low thermal resistance while at the same time minimizing parasitics. It is also shown that broad-band negative resistances can be generated without external feedback elements. This paper also reports experimental results where output powers of 390 mW with 22-percent efficiency at 8.5 GHz and 230 mW with 26-percent efficiency at 11.7 GHz have been demonstrated.**

I. INTRODUCTION

THE BEST performance reported to date for GaAs FET power oscillators operating above 8 GHz has been achieved using common-gate circuits with devices heat sunk through the SI GaAs substrate [1]–[6]. Typical common-gate single-frequency results are 500 mW at 9.0 GHz with 27-percent efficiency and 210 mW at 11.5 GHz with 17.5-percent efficiency [1]. Common-gate VCO circuits have achieved 40-percent bandwidth with YIG [4], [5] and varactor tuning elements [6]. Since GaAs is a relatively poor heat conductor, for power oscillator applications, the FET was either thinned and plated up with metal, or the device spread out to extract the heat generated. An alternate method for thermal management of power FET's is to operate the devices in a flip-chip format in which heat is removed from the surface of the chip where it is generated. This mounting procedure does not, however, lend itself to a common-gate configuration.

In this paper, GaAs FET oscillators using flip-chip mounted devices in a novel common-drain configuration will be described. This mode of operation has been referred to in the literature as a "reverse channel" circuit [8]. This oscillator type exploits the symmetry of self-aligned gate processing [7] and the performance properties of flip-chip mounted devices [9], [10]. It will be shown how common-drain oscillators can achieve low thermal resistance while at the same time minimizing parasitics which degrade high-frequency performance. It will also be shown that broad-band negative resistances can be generated simply without introducing external feedback elements, which can then be effectively used in oscillator applications. Using this approach, fixed-tuned power oscillators with output powers as high as 390 mW at 8.5 GHz with 22-percent efficiency and 230 mW at 11.7 GHz with 26-percent efficiency have been demonstrated. Varactor-tuned oscillators operating from 10.5 and 12.5 GHz with simple single-tuned networks have also been realized.

II. FLIP-CHIP FET'S

Flip-chip power FET's realize low chip-to-carrier thermal resistance while at the same time minimizing source parasitic inductance. This section will review briefly flip-chip considerations and will show how the same device may be operated in either a common-source or common-drain configuration by simply reversing the source-to-drain bias polarity. Measurements from 4 to 12 GHz

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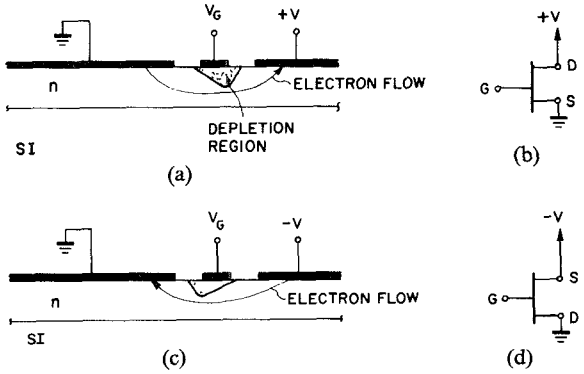


Fig. 1. Biased FET structure and circuit representation. (a) Common source. (b) Common drain.

indicate that this common-drain mode of operation is particularly suited for power oscillator applications.

A. Common-Source Operation

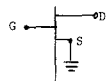
Fig. 1 is a simplified drawing of a depletion-mode FET comprised of two ohmic contacts separated by a Schottky-barrier junction. In a common-source configuration (Fig. 1(a)), one ohmic contact is defined to be the source and the other contact as the drain. For an n-type active region, the drain is biased to a positive potential with respect to the source, and the gate contact is made negative with respect to the source. The corresponding electron flow is from the source to the drain, and the depletion area under the gate is larger in the higher field drain region. For RCA flip-chip FET's [9], [10], the source (which is larger than the drain) is plated up with posts above the surface of the chip while the gate is symmetrically located between the source and drain. Fig. 1(b) is the corresponding circuit representation for a common-source FET.

For a flipped device, leads are first attached to the gate and drain contacts. The device is then flipped onto a copper pedestal which makes simultaneous connections to all plated-up sources. The gate and drain leads are then connected to the circuit. In a common-source configuration, most of the heat is generated near the drain where the electric field is a maximum. Since the sources are directly connected to a grounded copper pedestal, the shortest path for the heat generated near the drain is through the sources. It has been shown both experimentally and theoretically that this is an effective way to extract heat from the chip surface. For example, a 1-W device pattern with 16 150-μm gate-wide stripes has a total thermal resistance less than 25°C/W. It should also be noted that by attaching all sources directly to ground without bond wires, the source inductance is also minimized. The flip-chip construction, therefore, simultaneously minimizes both thermal resistance and parasitic source inductance.

B. Common-Drain Operation

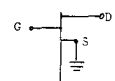
A common-drain circuit configuration may be realized using the same device pattern previously described by redefining the source and drain contacts and using a negative bias on the ungrounded terminal (Fig. 1(b)). In this case, electron flow is in the opposite direction, and the depletion region is larger near the grounded contact, which in this case is the drain. Therefore, by reversing the applied voltage to the ungrounded contact, a common-drain circuit configuration can be achieved with all the performance advantages previously described.

TABLE I
4–12-GHz Small-Signal Common-Source and Common-Drain S Parameters for Device 3100-1
Common Source: $V_{GS} = -1$ V; $V_{GS} = +8$ V



Freq. (GHz)	S (Magnitude and Angle) 11		21		12		22	
4	0.82	-106	1.87	88.4	0.090	12.0	.528	- 73.4
5	0.81	-121	1.54	73.0	0.089	- 0.5	.535	- 89.3
6	0.76	-127	1.28	62.3	0.086	- 8.9	.562	- 98.8
7	0.76	-132	1.09	53.3	0.088	-17.7	.587	-106.6
8	0.79	-137	1 06	45.5	0 076	-18 5	.633	-111.5
9	0.79	-142	1.02	37.4	0.093	-18.3	634	-116.2
10	0.76	-149	1.00	26.0	0.094	-32.3	.630	-123.8
11	0.81	-158	1.07	14.8	0.105	-40.1	.636	-134.6
12	0.77	-173	1.03	-2.0	0.104	-55.6	.574	-147.3

TABLE II
4–12-GHz Small-Signal Common-Source and Common-Drain S Parameters for Device 3100-1
Common Drain: $V_{GD} = -9$ V; $V_{SD} = -8$ V



Freq (GHz)	S (Magnitude and Angle) 11		21		12		22	
4	0.93	- 70 4	1.03	-49 5	0.32	30.2	.19	145.3
5	0 93	- 87 8	0.93	-61 9	0 35	16.0	.17	161.1
6	0.86	- 97.4	0.83	-69 8	0.37	5 1	16	-177.0
7	0.87	-103.8	0.75	-74.3	0.39	- 3.7	.19	-159 0
8	0 89	-110.3	0.71	-80.7	0.41	-10.2	.20	-155.3
9	0.86	-113 4	0.69	-84.3	0.45	-15.4	.16	-153.5
10	0.86	-117.5	0.69	-92.7	0 49	-27 2	.14	-151.8
11	0.919	-118.1	0.72	-94 3	0.56	-31 3	.11	-159.6
12	0.925	-131 7	0.74	-108.1	0 61	-48.0	.05	-176.2

C. Circuit Characterization

Tables I and II summarize the common-source and common-drain small-signal S-parameter measurements for an RCA FET. The gate length and gate width for this device type are 1 and 600 μm, respectively. With the source grounded, this transistor has a maximum unilateral gain of 7.8 dB at 12 GHz and is stable under all source and load conditions over the frequency 4–12-GHz range. With the drain grounded, the S parameters change significantly. There is an overall redistribution of the S parameters; in particular, there is a dramatic increase in the feedback term (S_{12}). At 12 GHz the magnitude of the common-drain feedback term increases by a factor of 5.8 over the common-source value. The feedback is so large that the stability factor (K) is less than unity over the entire measured frequency range.

III. Single-Frequency Oscillator Results

Single-frequency oscillators have been built and tested using devices with 600- and 1200-μm total gate width. These oscillators have a resonator on the gate side which

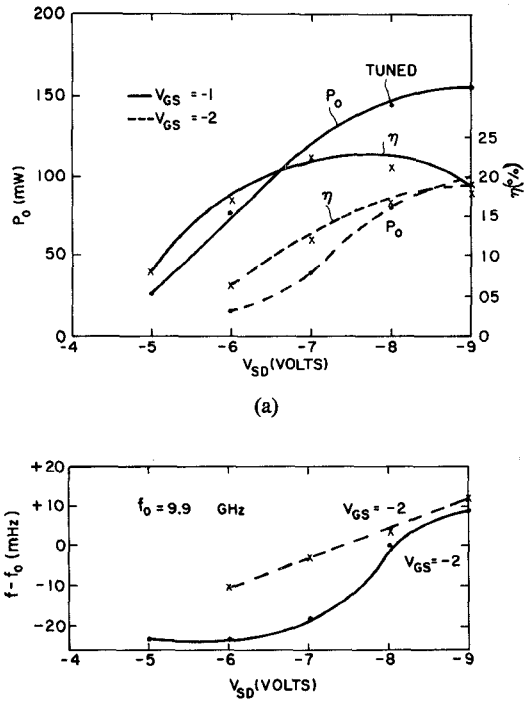


Fig. 2. 600-μm gate-width power oscillator performance. (a) Output power and efficiency. (b) Frequency change with bias variations.

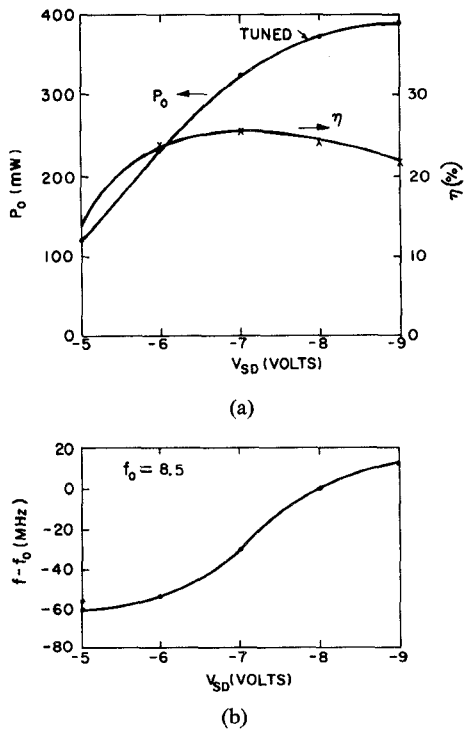


Fig. 3. 1200-μm gate-width power oscillator performance. (a) Output power and efficiency. (b) Frequency change with bias variations.

consists of the device gate capacitance and an inductor realized with bond wires from the carrier gate pad to a grounded bypass capacitor. The value of the inductor is chosen to resonate the device gate capacitance at the desired center frequency. This may be varied by adding or subtracting wire bonds. On the source side, a tuner is used to cause the device to oscillate.

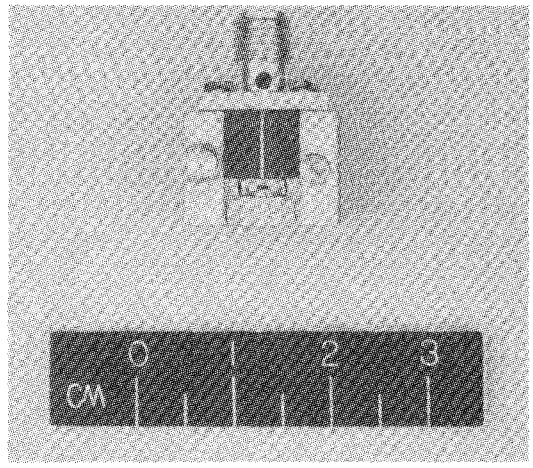


Fig. 4. Photograph of a common-drain voltage-controlled oscillator.

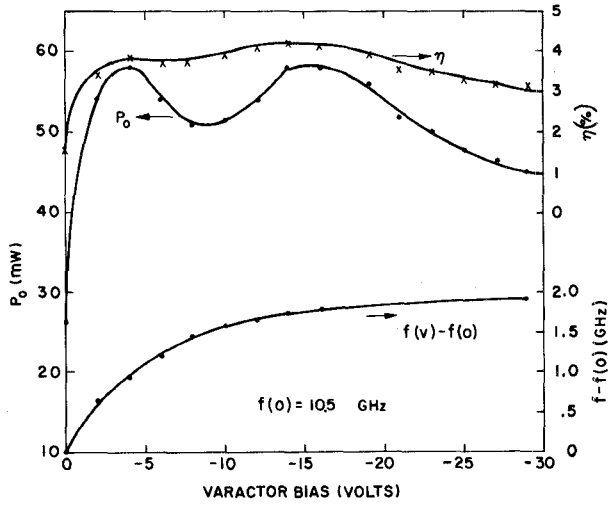


Fig. 5. Common-drain oscillator VCO performance.

Using this approach, oscillators in the 8–12-GHz frequency range have been studied. The oscillator circuit is considered to consist of the device, gate resonator, and output tuner (including tuner losses). Fig. 2(a) and (b) are plots of output power, efficiency, and frequency change for an oscillator using a 600-μm gate-width device. This device was tuned at 9.9 GHz, and at this point the output power was 150 mW and the efficiency 22 percent. The performance as a function of bias variations was measured with the fixed tuning. Fig. 3(a) and (b) are similar curves for a 1200-μm gate-width FET. With a source–drain voltage of 8 V, the output power is 370 mW at 8.5 GHz with an efficiency of 24 percent. At a source–drain voltage of 7 V, the efficiency increases to 26 percent with a slight sacrifice in output power (325 mW). Using similar techniques, a 1200-μm wide device achieved 230 mW at 11.7 GHz with 26-percent efficiency.

IV. Voltage-Controlled Oscillators

By placing a varactor in the gate circuit and presenting the necessary source impedance to the FET, voltage tunable common-drain oscillators were realized. Fig. 4 is a photograph of a common-drain voltage-controlled oscillator tunable over the 10.5–12.5-GHz band. For this oscilla-

tor the gate resonant circuit is a lumped element series resonant arrangement consisting of chip varactor, series wirebond, and the gate input impedance. The output drain circuit is a single section impedance transformer. Fig. 5 shows the tuning characteristic of this oscillator. The minimum output power and efficiency are 25 mW and 1.6 percent, respectively. Over most of the tuning range, the output power is in excess of 40 mW and the efficiency is greater than 3 percent.

V. Conclusions

It has been shown that, in a symmetrical FET structure, the roles of the source and drain ohmic contacts may be interchanged by reversing the source–drain bias polarity. In power oscillator applications, this allows the realization of an optimally heat-sunk flip-chip common-drain circuit. Using this technique, both single-frequency and varactor-tuned high-frequency oscillators have been realized. It is felt that this technique will find wide usage in microwave oscillators because of the simplicity of the approach and the high performance possible.

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11-GHz GaAs Power MESFET Load-Pull Measurements Utilizing a New Method of Determining Tuner *Y* Parameters

HIROYUKI ABE AND YOICHI AONO

***Abstract*—A load-pull technique utilizing a new method of determining tuner *Y* parameters is proposed for large-signal characterization of microwave power transistors. Large-signal input–output transfer characteristics of an active circuit containing a GaAs FET and an input matching circuit are measured by inserting a microstrip tuner between the active circuit output drain terminal and the 50-Ω load. The microstrip-tuner *Y* parameters are determined by comparing the dc bias-dependent small-signal *S* parameter S_{22} of the active circuit and that of the circuit which contains the active circuit and microstrip tuner. The reflection coefficient presented to the active circuit output drain terminal is derived from tuner *Y* parameters.**

Optimal load impedances for output power, obtained with this new load-pull technique, are used to design *X*-band GaAs FET power amplifiers. An 11-GHz power amplifier with a 3000-μm gate-width FET chip delivers 1-W microwave power output with 4-dB gain in the 500-MHz band.

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I. Introduction

IN DESIGNING power amplifiers, it is important to know the transistor load characteristics at a high input driving-power level and to optimize the output matching

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